**Amendments to the Specification:**

Please replace the third paragraph on page 1 with the following amended paragraph:

As a consequence of the separation of the protocol controller and the transceiver, information between the two must be exchanged via an interface. To this end, a transmission line is provided by means of which the protocol controller informs the transceiver that a writing process should be performed on the bus. Conversely, the transceiver on a receiving line signals ~~signalizes~~ that it has received data on the bus. Such a construction is provided, for example, in many transceivers and protocol controllers for the controller area network (CAN) ~~CAN~~ bus which is particularly used in vehicles.

Please replace the fourth paragraph on page 2 with the following amended paragraph:

A transceiver for a serial data bus, in which the transceiver is connected via a transmission line and a receiving line to a protocol controller which manages a data bus protocol, and is coupled to the lines of the data bus, and in which the transceiver comprises means for error management which supply an error signal when they recognize that the data bus lines are active and when the receiving line simultaneously signals ~~signalizes~~ an inactive bus, said error signal having the effect that the transceiver no longer acts actively on the data bus.

Please replace the fifth paragraph on page 2 with the following amended paragraph:

This first embodiment of the invention provides a solution for the erroneous situation when the receiving line (RXD) is permanently clamped to the inactive state. In such a case, the protocol controller would start transmitting to the data bus at arbitrary instants, assuming that the bus is free. Possible transmissions on the data bus are thereby eliminated and the availability of the bus system is limited until complete rejection. To avoid this, means for error management are provided in the transceiver in accordance with the first embodiment of the invention. These means check whether data bus lines are simultaneously active and whether the receiving line signals ~~signalizes~~ an inactive bus. This would exactly be the erroneous situation described above, in which the data line is clamped to the inactive state but in which actually the data bus is active. In this case, the means for error management according to the invention prevent the

data bus from being used by the protocol controller or the transceiver, in that the means for error management supply an error signal which has the effect that the transceiver no longer acts actively on the data bus, thus sends no dominant bits to the data bus. It is thereby ensured for the erroneous situation described above that, due to inactive clamping of the receiving line, the transceiver or the protocol controller can no longer transmit data to the bus and thus do not destroy data communication which is taking place on the bus. It is particularly advantageous that the error state is already recognized before the communication on the bus is affected.

Please replace the second paragraph on page 3 with the following amended paragraph:

A transceiver for a serial data bus, in which the transceiver is connected via a transmission line and a receiving line to a protocol controller which manages a data bus protocol, and is coupled to the lines of the data bus, and in which the transceiver comprises means for error management, which means comprise a timer circuit which triggers an error signal when the transmission line is active for a longer period than a predetermined time interval, said error signal having the effect that the transceiver no longer acts actively on the data bus, which error signal is cancelled only when the transmission line signals ~~signalizes~~ an inactive bus and the receiving line signals ~~signalizes~~ an active bus.

Please replace the fifth paragraph on page 3 with the following amended paragraph:

In accordance with the second embodiment of the invention, this problem is solved in that the transceiver according to the invention comprises means for error management, which means trigger an error signal when the transmission line is active for a longer period than a predetermined time interval, said error signal having the effect that the transceiver no longer acts actively on the data bus. In contrast to the state of the art, this error signal is, however, not cancelled in dependence upon time but persists until the transmission line signals ~~signalizes~~ an inactive bus and the receiving line signals ~~signalizes~~ an active bus.

Please replace the first paragraph on page 4 with the following amended paragraph:

In the solution according to the invention, it is ensured that the error signal is not cancelled until after it is certain that the erroneous state has been eliminated. This is the case when, on the

one hand, the receiving line signals ~~signalizes~~ an active bus but, on the other hand, the transmission line is inactive.

Please replace the second paragraph on page 4 with the following amended paragraph:

In accordance with an embodiment of the invention for the first embodiment as defined in claim 3, the error signal is switched off when the receiving line signals ~~signalizes~~ an active bus. In this case it is ensured that clamping of the receiving line to the inactive state is cancelled and that the disturbance is eliminated.

Please replace the fourth paragraph on page 4 with the following amended paragraph:

As is also common for both embodiments, a further embodiment of the invention as defined in claim 5 is characterized in that the error signal is signaled ~~signalized~~ to the exterior via an error line. This is particularly advantageous for signaling ~~signalizing~~ the erroneous state to the protocol controller in order that this controller does not attempt further transmissions, and for the purpose of informing an application about the erroneous bus state.

Please replace the sixth paragraph on page 5 with the following amended paragraph:

The block diagram in the Figure further shows a differential amplifier 7 whose inverting output in state 0 signals ~~signalizes~~ when the data bus, i.e. the two data bus lines 2 and 3, is recessive. However, when the differential amplifier 7 supplies a signal with a high level, it signals ~~signalizes~~ that a dominant bit is transmitted on the data bus. This signal is signaled ~~signalized~~ on a receiving line RXD via a push-pull driver stage comprising two transistors 8 and 9. This receiving line is particularly evaluated by the protocol controller (not shown). The protocol controller thus knows at any time via the signal received on the receiving line RXD which processes take place on the data bus and on data bus lines 2 and 3.

Please replace the first paragraph on page 6 with the following amended paragraph:

The fact that the receiving line RXD is permanently clamped to the inactive state may be such an error. In this case, the protocol controller would assume that the data bus is free and would attempt to transmit. However, when data communication already takes place simultaneously on

the data bus, this would be severely disturbed and might lead to complete interruption of the data communication. To recognize this erroneous case, a first embodiment of the invention is characterized in that an error signal is generated when the means 1 for error management recognize that the data bus lines are active but the receiving line RXD simultaneously signals ~~signalizes~~ an inactive bus. This case would occur, for example, when the receiving line is clamped to the inactive state.

Please replace the fourth paragraph on page 6 with the following amended paragraph:

The output signal of the time filter 12 is applied to a D flip-flop 14 via an OR gate 13. This signal is applied to a set input S of the D flip-flop. An output of the D flip-flop supplies an error signal F. This error signal F is applied to the transmitter 4 and is signaled ~~signalized~~ on external components via an error line ERR, for example, on the above-mentioned protocol controller (not shown).

Please replace the second paragraph on page 7 with the following amended paragraph:

This circuitry of the means 1 for error management covers the case where the data bus lines are active but where the receiving line simultaneously signals ~~signalizes~~ an inactive data bus. This case may occur, for example because the receiving line is clamped to the inactive state. In this erroneous case, the first AND gate 11 would supply a corresponding output signal which would have the result that the D flip-flop would be set via the filter 12 and the OR gate 13. When the D flip-flop 14 is set, it supplies an error signal which has the effect that an erroneous case is signaled ~~signalized~~ to the transmitter 4. In this case, the transmitter 4 switches the transmission stages 5 and 6 to the inactive state so that data communication that may be taking place between other participants on the data bus lines 2 and 3 is not disturbed. Furthermore, this error signal is signaled ~~signalized~~ to the protocol controller (not shown) via the error line ERR, so that this controller does not undertake any further transmission attempts.

Please replace the second paragraph on page 8 with the following amended paragraph:

The second AND gate 17 supplies an output signal when the transmission line is inactive and the receiving line is active. In this case, the signal is again applied to a reset input of the D flip-flop 14 via a filter 18 for the purpose of compensating delay times. The D flip flop 14 is thus

reset again under the above-mentioned condition so that the error signal F is switched to the inactive state again. This is signaled ~~signalized~~ to the protocol controller via the error line ERR. Simultaneously, the transmitter 4 will switch the driver stages 5 and 6 to the active state again in so far as a corresponding transmission takes place through line TXD.